CLAIMS

What is claimed is:

1. A method of fabricating a semiconductor device, the method comprising:

forming a gate on a semiconductor substrate, the gate including opposing side surfaces;

depositing an oxide material over the gate electrode and the semiconductor substrate, the opposing side surfaces of the gate being substantially free of the oxide material; and

forming spacers on the opposing side surfaces of the gate, the spacers contacting the opposing side surfaces of the gate substantially along the opposing side surfaces.

2. The method of claim 1, the gate being doped with p-type or n-type dopant.

3. The method of claim 2, the sidewall spacers mitigating diffusion of dopants from the opposing side surfaces of the gate.

4. The method of claim 1, the oxide material being deposited by physical vapor deposition.

5. The method of claim 4, the physical vapor deposition method being anisotropic.

6. The method of claim 4, the physical vapor deposition method comprising at least one of a collimated sputtering method, a long throw sputtering method, or an ionized metal plasma sputtering method.

7. The method of claim 1, the oxide material comprising at least one of SiO_2, AlO_3, ZrO_2, HfO_2 (AlHf) O_X, HfO_2, La_2O_3, Y_2O_3, silicon oxynitride, or hafnium silicon oxynitride.

8. The method of claim 1, the formation of the spacers further comprising providing a nitride layer over the gate after depositing the oxide material; and

etching the nitride layer.

9. The method of claim 8, further comprising implanting an LDD implant after forming the gate, but before depositing the oxide layer; and

implanting a source/drain implant after forming the nitride spacers.

10. The method of claim 9, the LDD implant and the source/drain implant forming a source region and a drain region of the semiconductor device.

11. The method of claim 10, the gate forming part of a p-type metal oxide semiconductor (PMOS) structure.

12. A method of fabricating a semiconductor device, the method comprising:

forming a gate on a semiconductor substrate, the gate being doped and including opposing side surfaces;

depositing an oxide material over the gate and the semiconductor substrate, the opposing side surfaces of the gate being substantially free of the oxide material;

forming a nitride layer over the gate and the oxide material; and

etching the nitride layer to form nitride spacers on the opposing side surfaces of the gate, the nitride spacers contacting the opposing side surfaces of the gate substantially along the opposing side surfaces.

13. The method of claim 12, the nitride spacers mitigating diffusion of dopants from the opposing side surfaces of the gate.

14. The method of claim 12, the oxide material being deposited by physical vapor deposition.

15. The method of claim 14, the physical vapor deposition method comprising at least one of a collimated sputtering method, a long throw sputtering method, or an ionized metal plasma sputtering method.

16. The method of claim 12, the oxide layer comprising at least one of SiO_2, AlO_3, ZrO_2, HfO_2 (AlHf) O_X, HfO_2, La_2O_3, Y_2O_3, silicon oxynitride, or hafnium silicon oxynitride.

17. The method of claim 12, the gate comprising a polysilicon material doped with a p-type dopant.

18. The method of claim 12, further comprising:

implanting a LDD implant after forming the gate, but before depositing the oxide layer; and

implanting a source/drain implant after forming the nitride spacers.

19. The method of claim 12, the gate forming part of semiconductor device comprising a PMOS structure.

20. A semiconductor device comprising:

a semiconductor substrate

a gate formed on the semiconductor substrate, the gate including opposing side surfaces, and

spacers contacting the opposing side surfaces of the gate electrode substantially along the opposing side surfaces, the opposing side surfaces of the gate electrode being substantially free of a material that depletes the dopant from the gate electrode.

21. The semiconductor device of claim 20, the gate comprising polysilicon doped with a p-type dopant.

22. The semiconductor device of claim 21, the spacers comprising a nitride material.

23. The semiconductor device of claim 22, the semiconductor substrate further comprising source and drain regions, the source and drain regions defining a channel, the gate overlying the channel.